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10/765,406	01/26/2004	Darrell Rinerson	UNTYP030	2199

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,406	RINERSON ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42,44 and 45* is/are rejected.

7)☒ Claim(s) *43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 01/26/2004 is acceptable.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "refractory interconnect metal layers in-between the substrate and the bottom refractory metal layers" of **claim 22,** "interconnect metal layers above the top metal layer" of **claims 23**, and "a plurality of contact plugs that are stable at the high temperature are formed beneath the multi-resistive state element" of **claim 32** must be shown or the feature(s) canceled from the claim(s). Similarly, the limitations "electrode", "barrier layer", "sacrificial layer", and "non-ohmic device" of **claims 10, 39, 43, 11, 15, 38, and 43** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim(s) **15** is/are objected to because it/they contain(s) typographical errors:

- **Claim 15**, line 1 recites:

"claim 1"

which should be:

"claim 10"

because claim 10 recites "an electrode" as an antecedent basis for "the electrode" of claim 15.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 25-29** are rejected under 35 U.S.C. 102(e) as being anticipated by Slaughter et al. U.S. Patent 6,544,801 (the '801 patent).

The '801 patent discloses in the figures, particularly Figure 5-7, and respective portions of the specification a memory and an inherent method of manufacturing thereof as claimed.

Referring to **claim 25**, the '801 patent discloses a memory, comprising:

a substrate (20 or 52);

a memory array (column 2, lines 42-45) that includes a plurality of memory cells (only one cell is shown in the figures), each memory cell including a multi-resistive state element (24...28 or 56...67) , the multi-resistive state element being above the substrate and being formed with a high-temperature fabrication process at a high temperature (column 4, first paragraph, and high temperature processing is interpreted at about 400 °C);

a plurality of conductive lines (22 or 54, however, only one line is shown) beneath the multi-resistive state element, the plurality of conductive lines (for example, copper, column 4, lines 40-46, and visit http://www.chemicalelements.com/elements/xx.html with xx being the metal symbol, for copper melting point which is about 1083.0 °C), being stable (stable is interpreted broadly) at the high temperature (about 400 °C); and

a plurality of conductive lines (29 or 68, for example aluminum, column 4, lines 40-46) above the multi-resistive state element.

Referring to **claim 26**, the '801 patent further discloses that the plurality of conductive lines above the multi-resistive state element are not stable at the high temperature (when the plurality of conductive lines above the multi-resistive state element is formed of aluminum, out of the group of aluminum or copper as cited above, which has a melting point of about 660.37 °C, which is not stable at about 400 °C, wherein "stable" is interpreted broadly).

Referring to **claim 27**, the '801 patent further discloses that the multi-resistive state element (MTJ cell) is re-writable.

Referring to **claims 28 and 29**, the '801 patent further discloses a plurality of electrodes (72, 74, Fig. 7, 72 being "metalization layer", for example, copper, and 74 "diffusion barrier",

column 5, last paragraph) that are stable at the high temperature are formed beneath the multi-resistive state element, and that each of the plurality of electrodes includes a barrier layer (74).

Claim Rejections - 35 USC § 102 and 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1-6, 8-9, 25-27, 33-35, 37, and 44** are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Hsu et al. U.S. Patent 6,693,821 (the '821 patent).

The '821 patent discloses in the figures and respective portions of the specification a memory and an inherent method of manufacturing thereof but fails to disclose a few properties as claimed.

Specifically with reference to **claim 1**, the '821 patent discloses a cross point memory (Figs. 5 and 6), comprising:

a substrate (12) having a deposition face;

a memory array that includes a plurality of memory cells;

a bottom refractory metal layer (platinum, in a preferred embodiment, column 2, lines 30-35) that has a melting point (of about 1,772 °C), parallel to the deposition face of the substrate, patterned into bottom conductive array lines (14); and

a top metal layer, parallel to the deposition face of the substrate, patterned into top conductive array lines (18) such that a memory cell may be at least partially defined by the intersection of a bottom conductive array line and a top conductive array line, the memory cell capable of being programmed by application of voltages on the bottom conductive array line and the top conductive array line (as is known in the art of electrically programmable resistance cross-point memory in the instant case or in the art of memory in general).

However, the reference fails to disclose that at least a portion of the memory cell is formed using high temperature processing at a first temperature and further fails to disclose that the melting point of platinum (bottom refractory metal) is above the first temperature.

Nevertheless, the missing properties is either anticipated, if "high temperature processing" is interpreted broadly, or obvious or inherent, since the '821 patent discloses that the memory material 17 is a perovskite material and is preferably a colossal magnetoresistive (CMR) material or a high temperature superconducting (HTSC) material, for example Pr.sub.0.7 Ca.sub.0.3 MnO.sub.3 (PCMO), Gd.sub.0.7 Ca.sub.0.3 BaCo.sub.2 O.sub.5 (column 2, lines 40-50), depending on how, again, one interprets "high temperature processing". For an example of high temperature processing of perovskite materials, see U.S. Patent 6,730,575 to Eldridge et al. which specifies a range of about 600-700 °C, and an example of high temperature superconducting (HTSC) material, see U.S. Patent 6,794,052 to Schultz et al., which specifies a range of about 800-1000 °C (column 26, last paragraph).

Referring to independent **claim 25** and using the same reference characters and citations and interpretations as detailed above where applicable, the '821 patent discloses a memory, comprising:

a substrate;

a memory array that includes a plurality of memory cells, each memory cell including a multi-resistive state element ("resistive memory"), the multi-resistive state element being above the substrate and being formed with a high-temperature fabrication process at a high temperature (for example, 600 °C);

a plurality of conductive lines beneath the multi-resistive state element; and

a plurality of conductive lines above the multi-resistive state element.

However, the reference fails to disclose that the plurality of conductive lines (platinum) beneath the multi-resistive state element is stable at the high temperature. Nevertheless, it would appear that platinum, which has a melting point of about 1,772 °C, would be stable at about 600 °C).

Referring to independent **claims 33 and 44** and **claim 26**, and using the same reference characters and citations and interpretations as detailed above where applicable, the '821 patent discloses a memory, comprising:

a substrate;

a plurality of circuits on the substrate;

a plurality of x-direction lines (14) in a first metal layer (platinum) parallel to the substrate, with the x-direction lines oriented in one direction;

a plurality of y-direction lines (18) in a second metal layer (for example, copper, column 2, lines 57-62) above the first metal layer, with the y-direction lines oriented in a different direction as the x-direction lines, and crossing the x-direction lines; and

a plurality of memory plugs (22, Fig. 4) located substantially at the intersections of the x-direction lines and y-direction lines, and in-between the first and second metal layers.

However, the reference fails to disclose that wherein the memory plugs have at least one layer that requires a minimum temperature for fabrication and thus fails to disclose that the first metal layer (platinum) is a metal with a melting point (1,772 °C) above the minimum temperature required for fabrication and further fails to disclose that the second metal layer (copper) is a metal that is not stable at the minimum temperature required for fabrication.

Nevertheless, as mentioned above, it appears that a minimum temperature for fabrication for perovskite, a layer of memory plug 22, is about 600 °C, and it would follow that platinum, which has a melting point of about 1,772 °C, would be stable at about 600 °C, and copper, which has a melting point of about 1083.0 °C, would not be stable at the minimum temperature required for fabrication of about 600 °C).

Referring to **claims 2 and 27**, the resistance of the '821 patent's nonvolatile, multi-resistive state magnetoresistive memory cells can be reversibly programmed to different values and re-writable.

Referring to **claim 3**, the complex metal oxides 17 of the memory cells listed in column 2, lines 40-50, include a conductive metal oxide.

Referring to **claim 4**, the '821 patent further discloses that the memory cells includes a crystalline or poly-crystalline material (perovskite material 17).

Referring to **claims 5 and 37**, the top metal layer (18, formed of copper, as detailed above) is not a refractory metal and that the second metal (18, formed of copper, as detailed above) is copper.

Referring to **claim 6**, the top metal layer (copper) meets the limitation of the Markush group of copper or an aluminum alloy.

Referring to **claim 8**, as mentioned above, the bottom refractory metal layer has a melting point of at least 700 °C.

Referring to **claim 9**, as mentioned above, the bottom refractory metal layer appears to be stable at 600 °C.

Referring to **claim 34**, the first metal (platinum) is a refractory metal.

Referring to **claim 35**, the second metal (copper) does not appear to be capable of sustaining processing temperature above 450 °C.

6. **Claims 1-4, 8-9, 24-25, and 27** are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Hsu et al. U.S. Patent 6,569,745 (the '745 patent).

The '745 patent discloses in the figures and respective portions of the specification a memory and an inherent method of manufacturing thereof but fails to disclose a few properties as claimed. The rejections claims **1-4, 8-9, 25, and 27** are similar to those of the '821 patent, cited above - because the '745 patent is about a 3-D version of the device and method of fabricating thereof of the '821 patent – therefore is not repeated here.

Referring to **claim 24**, the '745 patent further discloses that there are at least 2 memory arrays, whereby the at least 2 memory arrays are stacked upon one another (Figs. 1-11, particularly Fig. 1).

7. **Claims 1-23, 25-31, 33-42, and 44** are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ignatiev et al. U.S. Patent 6,473,332 (the '332 patent).

The '332 patent discloses in Fig. 1 and respective portions of the specification a memory and an inherent method of manufacturing thereof but fails to disclose a few properties as claimed.

Specifically with reference to **claim 1**, the '332 patent discloses a cross point memory (column 2, line53: "in a column-row or array format"), comprising:

a substrate (104) having a deposition face;

a memory array that includes a plurality of memory cells (only one cell is shown);

a bottom refractory metal layer (such as platinum (Pt), column 7, lines 10-16) that has a melting point, parallel to the deposition face of the substrate, patterned into bottom conductive array lines (generally referred to as 108. Note that 108 is called "electrode"; however, since the '332 patent discloses utilizing the cell 102 of Fig. 1 in "a column-row or array format" and further discloses in column 7, line 10: "[S]uitable electrode materials include, without limitation, metals, metallic oxides, polymers, or mixtures or combinations thereof. Exemplary examples of are, but not limited to, Pt, Ag, Au, LaSrCoO.sub.3, YBa.sub.2 Cu.sub.3 O.sub.7-x, RuO.sub.2, IrO.sub.2, SrRuO.sub.3, Al, Ta, TaSiN, MoN doped polyacetylene, polypyrrole, polyaniline, or any other "intrinsically conductive polymers" (ICP), or mixtures or combinations thereof" and in column 8, line 14: "resistance element material layer, electrodes and buffer layers (if needed) can be grown by pulsed laser deposition (PLD), sputtering, metal organic chemical vapor deposition

(MOCVD), chemical vapor deposition (CVD), MOD", it follows that conductive array lines are inherent from the disclosure); and

a top metal layer, parallel to the deposition face of the substrate, patterned into top conductive array lines (112, and same interpretation as for the bottom metal layer) such that a memory cell may be at least partially defined by the intersection of a bottom conductive array line and a top conductive array line, the memory cell capable of being programmed by application of voltages on the bottom conductive array line and the top conductive array line (as is known in the art of electrically programmable resistance cross-point memory in the instant case or in the art of memory in general).

However, the reference fails to disclose that at least a portion of the memory cell is formed using high temperature processing at a first temperature and further fails to disclose that the melting point of the bottom metal, a refractory metal such as platinum from the list of suitable materials cited above, is above the first temperature.

Nevertheless, the missing properties is either anticipated, if "high temperature processing" is interpreted broadly, or obvious or inherent, since the '332 patent discloses that the memory material 110 is selected from complex metal oxides, which are similar to those detailed in the description of the present invention (column 8, lines 14-25). It follows that complex metal oxides require or appear to require high temperature processing.

Referring to independent **claim 25** and using the same reference characters and citations and interpretations as detailed above where applicable, the '332 patent discloses a memory, comprising:

a substrate;

a memory array that includes a plurality of memory cells, each memory cell including a multi-resistive state element ("electrically variable multi-state resistance computing"), the multi-resistive state element being above the substrate and being formed with a high-temperature fabrication process at a high temperature;

a plurality of conductive lines beneath the multi-resistive state element; and

a plurality of conductive lines above the multi-resistive state element.

However, the reference fails to disclose that the plurality of conductive lines (platinum for example) beneath the multi-resistive state element is stable at the high temperature. Nevertheless, it would appear that platinum, which has a melting point of about 1,772 °C, would be stable at about 600 °C).

Referring to independent **claims 33 and 44** and **claim 26**, and using the same reference characters and citations and interpretations as detailed above where applicable, the '332 patent discloses a memory, comprising:

a substrate;

a plurality of circuits on the substrate;

a plurality of x-direction lines (generally referred to as 108 as noted above) in a first metal layer (platinum) parallel to the substrate, with the x-direction lines oriented in one direction;

a plurality of y-direction lines (generally referred to as 112 as noted above) in a second metal layer (for example, aluminum (Al), from the list of suitable materials for the electrodes cited above) above the first metal layer, with the y-direction lines oriented in a different direction as the x-direction lines, and crossing the x-direction lines; and

a plurality of memory plugs ("resistance element material layer", generally referred to as 110, and see citation above) located substantially at the intersections of the x-direction lines and y-direction lines, and in-between the first and second metal layers.

However, the reference fails to disclose that wherein the memory plugs have at least one layer that requires a minimum temperature for fabrication and thus fails to disclose that the first metal layer (platinum) is a metal with a melting point (1,772 °C) above the minimum temperature required for fabrication and further fails to disclose that the second metal layer (aluminum) is a metal that is not stable at the minimum temperature required for fabrication.

Nevertheless, as mentioned above, it appears that a minimum temperature for fabrication for the resistive memory element 110, which is - as noted above - similar to the present invention's, would be similar to the present invention's, and therefore refractory metal platinum would be stable at the minimum temperature for fabrication, and aluminum, which has a melting point of about 660.37 °C, would not be stable at the minimum temperature required for fabrication.

Referring to **claims 2 and 27**, the resistance of the '332 patent's "electrically operated, overwritable, multivalued, non-volatile resistive memory element" (Abstract) can be reversibly programmed to different values and re-writable.

Referring to **claim 3**, the complex metal oxides 110 include a conductive metal oxide.

Referring to **claim 4**, the '332 patent further discloses that the memory cells includes a crystalline or poly-crystalline material (perovskite).

Referring to **claims 5 and 36**, the top metal layer (aluminum) is not a refractory metal and that the second metal (aluminum, metals, and mixtures and combinations thereof, as cited above) is an aluminum alloy.

Referring to **claim 6**, the top metal layer (aluminum alloy) meets the limitation of the Markush group of copper or an aluminum alloy.

Referring to **claim 7**, the bottom refractory metal layer (Ta (tantalum), selected from the list cited above) meets the limitation of the Markush group of tungsten, molybdenum or tantalum.

Referring to **claim 8**, as mentioned above, the bottom refractory metal layer has a melting point of at least 700 °C.

Referring to **claim 9**, as mentioned above, the bottom refractory metal layer appears to be stable at 600 °C.

Referring to **claim 34**, the first metal (platinum) is a refractory metal.

Referring to **claim 35**, the second metal (aluminum) does not appear to be capable of sustaining processing temperature above 450 °C.

Referring to **claim 10-23, 28-31, and 38-42**, although the reference does not explicitly and exactly disclose all possible combinations of the materials and layers as claimed, the citation above for the array, electrodes and buffer layers, resistive memory element and buffer layers, and furthermore, substrate and buffer layers (column 7, lines 46-60) meets or within the skill of one of worker in the art to select to meet. For example, the list of the suitable materials for the electrodes and buffer layers contains binary nitrides and ternary nitrides. Note also that

properties such as oxygen barrier of sacrificial oxygen barrier for the barrier layers or adhesive are derivable from the list of suitable materials cited above.

8. **Claims 1-2, 4, 24, and 33** are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Johnson et al. U.S. Patent 6,034,882 (the '882 patent).

The '882 patent teaches a three-dimensional (Fig. 5) memory having a state charge element 23 and a steering element 22 (Fig. 4a) that meets the limitations but fails to disclose a few properties as claimed.

Specifically with reference to **claims 1 and 24**, the '882 patent discloses a cross point memory (Fig. 5), comprising:

a substrate (not shown) having a deposition face;

a memory array that includes a plurality of memory cells;

a bottom refractory metal layer (generally referred to as 46, 460, or 406, Figs. 6, such as titanium silicide, column 12, lines 37-40, or molybdenum and tungsten, and column 14, lines 59-65) that has a melting point, parallel to the deposition face of the substrate, patterned into bottom conductive array lines (406); and

a top metal layer, parallel to the deposition face of the substrate, patterned into top conductive array lines (such as conductor 7, Fig. 5, or 48, Figs. 6's, using, for example, aluminum, column 14, lines 46-67) such that a memory cell may be at least partially defined by the intersection of a bottom conductive array line and a top conductive array line, the memory

cell capable of being programmed by application of voltages on the bottom conductive array line and the top conductive array line (as is known in the art of electrically programmable memory).

However, the reference fails to disclose that at least a portion of the memory cell is formed using high temperature processing at a first temperature and further fails to disclose that the melting point of the bottom metal, a refractory metal such as molybdenum, is above the first temperature.

Nevertheless, the missing properties is either anticipated, if "high temperature processing" is interpreted broadly, or obvious or inherent, since the '882 patent discloses that the memory component layers such as 40, 41,43 of Fig. 6a are polysilicon, and it is known that polysilicon is formed of a high temperature process. See, for example, U.S. Patent 6,424,565 to Brug et al., column 6, lines 40-45, for such a disclosure. It follows that polysilicon requires or appears to require high temperature processing.

Referring to independent **claim 33**, and using the same reference characters and citations and interpretations as detailed above where applicable, the '882 patent discloses a memory, comprising:

a substrate;

a plurality of circuits on the substrate;

a plurality of x-direction lines (25, Fig. 5) in a first metal layer (molybdenum) parallel to the substrate, with the x-direction lines oriented in one direction;

a plurality of y-direction lines (for example, 26) in a second metal layer (for example, aluminum) above the first metal layer, with the y-direction lines oriented in a different direction as the x-direction lines, and crossing the x-direction lines; and

a plurality of memory plugs (27, Fig. 5, 45, Fig. 6a) located substantially at the intersections of the x-direction lines and y-direction lines, and in-between the first and second metal layers.

However, the reference fails to disclose that wherein the memory plugs have at least one layer that requires a minimum temperature for fabrication and thus fails to disclose that the first metal layer (molybdenum) is a metal with a melting point (2,617 °C) above the minimum temperature required for fabrication and further fails to disclose that the second metal layer (aluminum) is a metal that is not stable at the minimum temperature required for fabrication.

Nevertheless, as mentioned above, it appears that a minimum temperature for fabrication for the polysilicon material would be "high", and refractory metal platinum would be stable even at the "high" minimum temperature for fabrication, and aluminum, which has a melting point of about 660.37 °C, would not appear to be stable at the high minimum temperature required for fabrication.

Referring to **claim 4**, the '882 patent further discloses that the memory cells includes a crystalline or poly-crystalline material ("polysilicon").

Claim Rejections - 35 USC § 103

9. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over the '821 patent for being obvious.

Although the '821 patent fails to disclose that the bottom refractory metal layer (platinum) is tungsten, molybdenum or tantalum, platinum is a refractory metal and is art-

equivalent to refractory tungsten, molybdenum or tantalum. See, for example, U.S. Patent 5,126,283 to Pintchovski et al., column 6, last paragraph, for such a disclosure.

10. **Claim 44** is rejected under 35 U.S.C. 103(a) as being unpatentable over the '745 patent in view of Furukawa et al. U.S. Patent 4,882,652 (the '652 patent).

The '745 patent discloses a memory and an inherent method of manufacturing thereof substantially as claimed and as detailed above for claims 1 and 25, including forming a bottom plurality of layers (bottom word lines 14) of a refractory metal such as platinum (column 3, lines 5-10) and forming a top plurality of layers (top word lines, or conductors, 22), but fails to disclose a specific material for the top plurality of layers. The '652 patent, in disclosing a semiconductor device, teaches that aluminum or copper is relatively inexpensive as compared with refractory metal platinum (Pt) or palladium (Pd) (column 6, lines 10-20) and can be used for conductors ("electrodes"). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '745 patent's top plurality of layers using aluminum or copper. One would have been motivated to make such a modification in view of the teachings by the '652 patent that aluminum and copper as conductors are relatively inexpensive (and in view of the lack of disclosure of materials of the '745 patent). And, as should be apparent by now, aluminum or copper, although a good and inexpensive conductor, is not stable at the first temperature, the temperature at which the multi-resistive state element is formed. In summary, since the '745 fails to specify a specific material for the top conductors ("top plurality of layers"), which failure amounts to about the same as teaching that any conductor is acceptable, and since the '652 patent teaches that aluminum or copper is an

inexpensive material for conductors, one would use copper or aluminum for the top conductor for economic benefits ("inexpensive"), with the unintended natural result (inherent) that the top conductor is not stable, which meets the claim limitation.

11. **Claim 32** is rejected under 35 U.S.C. 103(a) as being unpatentable over the '745 patent in view of Thomas U.S. Patent 5,414,301 (the '301 patent). **Claim 45** is rejected under 35 U.S.C. 103(a) as being unpatentable over the '745 patent in view of the '652 patent as applied above and further in view of the '301 patent.

The '745 patent or the '745 patent in view of the '652 patent discloses a memory and an inherent method of manufacturing thereof substantially as claimed and as detailed above for claims 1, 25, and 44, but fails to disclose that a plurality of contact plugs that are stable at the high temperature are formed beneath the multi-resistive state element (claim 32) and also fails to disclose that all of the metal layers below the topmost memory array are refractory metal layers and at least one metal layer above the topmost memory layer is not a refractory metal layer (claim 45).

As for the limitation "contact plugs" of claim 32, the '745 patent discloses that transistor structures or other components of a memory circuit may be formed prior to the formation of the memory array, which transistor structures or other components must be in electrical communication with the memory array through contact plugs as is known in the semiconductor art. In other words, for the '745 device to function, there must be contact plugs. And since the required contact plugs are formed prior to forming the memory array, the contact plugs are formed beneath the multi-resistive state element.

As for the limitation "not a refractory metal layer" in "at least one metal layer above the topmost memory layer is not a refractory metal layer" of claim 45, as noted above, the topmost word line, which is the equivalent of the claimed "at least one metal layer above the topmost memory layer" could be formed of aluminum or copper, and thus "not a refractory metal layer", for economic benefits.

As for the limitations "stable at the high temperature" in "contact plugs that are stable at the high temperature are formed beneath the multi-resistive state element" of claim 32 and "refractory metal layers" in "all of the metal layers below the topmost memory array are refractory metal layers", as shall be apparent by now from the references and interpretations, the '745 patent's resistive memory elements 17 or 27, formed of a complex metal oxide, CMR, or high temperature superconducting (column 3, lines 11-35) are formed by a high temperature process, and as detailed above, the bottom-most metal layers 14 are refractory metal layer.

What is missing from the '745 patent is the motivation for using a refractory (a material that has a high melting point) metal for the contact plugs (so that they are stable at the high temperature as claimed) and the motivation for using a refractory metal for all of the metal layers below the topmost memory array, where, just as mentioned, high temperature processes are conducted. The '301 patent, in disclosing a high temperature interconnect system for an integrated circuit, offers such a motivation by teaching that "a refractory metal or refractory metal compound with good stability over a barrier layer can be used to great advantage in high temperature processing" (the paragraph bridging columns 1 and 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '745 patent's device as claimed. One would have been motivated to make such a modification in

view of the teachings that refractory metals, which has high melting points and which are stable at high temperature, are suitable for high temperature processes, the processes by which the '745 patent's resistive memory elements are formed.

12. **Claims 24 and 45** are rejected under 35 U.S.C. 103(a) as being unpatentable over the '332 patent in view of Perner et al. U.S. Patent Application Publication 2003/0218902 (the '902 publication).

The '332 patent discloses a memory and an inherent method of manufacturing thereof substantially as claimed and as detailed above, including a disclosure for forming the memory in an array format and the variety of materials for the metal layers (electrodes) as claimed, but fails to disclose that the memory could be formed such that there are at least two arrays stacked upon one another as claimed. The '902 publication, in disclosing an MRAM device, which is also a resistive memory device, teaches in paragraph [0022] that stacking cells or arrays as shown in Figs. 1-5, can increase the data storage density of a memory ("data storage device"). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the '332 patent's memory so that, instead of forming just one level of memory array, the memory could be formed such that there are at least two arrays stacked upon one another. One would have been motivated to make such a modification in view of the teachings in the '902 publication that stacking arrays of memory can increase the data storage density.

Allowable Subject Matter

13. Claim 43 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a memory having **all** limitations as recited in **claim 33 and claim 43** characterized in an electrode that electrically connects the multi-resistive state element to the non-ohmic device. In particular, although the '882 patent discloses in Fig. 6a a non-ohmic device 40/41 and a multi-resistive state element (antifuse) 41/42/43, there is no motivation in the prior art of record to modify the structure to include an electrode that electrically connects the multi-resistive state element to the non-ohmic device.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 6,636,436 to Perner discloses an MRAM device wherein each cell comprises a horizontal oriented MTJ element and a vertical oriented non-ohmic isolation device (npn) in series with each other.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
December 09, 2004